

CLAIMS

- 1 1. An apparatus comprising:
- 2 a processor, coupled to a cache memory;
- 3 the cache memory with a plurality of cache lines, each cache line with at least one status
- 4 bit to represent whether the cache line contains a defect; and
- 5 a logic to perform at least one test of the plurality of cache lines and to set the status bit
- 6 for at least one of the plurality of cache lines.
- 1 2. The apparatus of claim 1 wherein the logic is a programmable built in self-test (PBIST) logic.
- 1 3. The apparatus of claim 1 wherein the logic is a plurality of scan chains and a test access port to accept automatic test pattern generation (ATPG) patterns.
- 1 4. The apparatus of claim 1 wherein the status bit is stored in a six-transistor static random access memory cell.
- 1 5. The apparatus of claim 1 wherein the status bit is stored in a register file cell.
- 1 6. The apparatus of claim 1 wherein the status bit is stored in a fuse.

1 7. The apparatus of claim '1 wherein the status bit is a read only bit during normal operation of
2 the system.

1 8. The apparatus of claim 1 wherein the cache memory is either one of a level 0 (L0) cache,
2 level 1 (L1) cache, or level 2 (L2) cache.

1 9. The apparatus of claim 2 wherein the PBIST logic can set the status bit during initialization of
2 the cache memory.

10. An article comprising:
 a storage medium having stored thereon instructions, that, when executed by a computing
 platform, result in execution of testing a processor's cache memory with a plurality of cache
 lines;
 generating a test pattern;
 stimulating the cache memory with the test pattern; and
 writing to at least one status bit for each cache line to indicate whether the cache line contains
 a defect.

1 11. The article of claim 10 wherein the cache memory is either one of a level 0 (L0) cache,
2 level 1 (L1) cache, or level 2 (L2) cache.

1 12. The article of claim 10 wherein the status bit is stored in either one of a six-transistor
2 static random access memory cell, a register file cell, or a fuse.

1 13. The article of claim 10 wherein the status bit is a read only bit during normal operation of
2 the cache memory.

1 14. A method of configuring a cache memory with a plurality of cache lines comprising:
2 testing the plurality of cache lines;
3 setting a status bit for at least one cache line to indicate whether the cache line has a
4 defect as a result of the testing; and
5 disabling the cache lines when the status bit indicates the defect.

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15. The method of claim 14 wherein the setting a status bit comprises storing the bit in either
one of a six-transistor static random access memory cell, a register file cell, or a fuse.

16. The method of claim 14 wherein the status bit is stored in either one of a six-transistor
static random access memory cell, a register file cell, or a fuse.

1 17. The method of claim 14 wherein the status bit is a read only bit during normal operation
2 of the cache memory.